



# PRODUCT SPECIFICATION

**MODEL: 208107002180590-06**

<◇> PRELIMINARY SPECIFICATION

<◆> APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED
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## 1. GENERAL DESCRIPTION

### 1.1 DESCRIPTION

2081070180590-06 is a color active matrix thin film transistor(TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This module is composed of a TFT LCD panel, driver ICs, FPC and a Backlight unit.

### 1.2 FEATURES:

No.	Item	Specification	Unit
1	Panel Size	7"	inch
2	Number of Pixels	1024(H) × 3(RGB) ×600(V)	pixels
3	Active Area	154.2144 (W) × 85.92(H)	mm
4	Pixel Pitch	0.1506(W) × 0.1432(H)	mm
5	Outline Dimension	163.8(W)×97(H)×2.8(T)	mm
6	Pixel arrangement	RGB vertical stripe	-
7	Display Mode	Normally White	-
8	Viewing Direction	6.0 o'clock	-
9	Display Color	16.7M	-
10	Luminance(cd/m2)	280(TYP.)	nit
11	Contrast Ratio	300(TYP.)	-
12	Surface Treatment	Anti-Glare	-
13	Interface	TTL	-
14	Backlight	White LED	-
15	Operation Temperature	0~50	℃
16	Storage Temperature	-10~60	℃
17	Weight	90.8(± 10%)	g



Technical drawing of a 1024x600 TFT LCD module. The drawing includes a top view showing the active area, bezel, and pin connections. Dimensions are provided in millimeters. A detailed view of the pin connections is shown at the bottom right. The drawing is labeled with 'FRONT' and 'BACK' views. A table of pin numbers and symbols is provided at the bottom left.

Pin numbers and symbols:

PIN	SYMBOL
1	A
2	A
3	K
4	K
5	GND
6	VCOM
7	VDD
8	MODE
9	DE
10	VS
11	HS
12	B7
13	B6
14	B5
15	B4
16	B3
17	B2
18	B1
19	B0
20	G7
21	G6
22	G5
23	G4
24	G3
25	G2
26	G1
27	G0
28	R7
29	R6
30	R5
31	R4
32	R3
33	R2
34	R1
35	R0
36	GND
37	DCLK
38	GND
39	L/R
40	UPIN
41	VGH
42	VGL
43	AVDD
44	RESET
45	NC
46	VCOM
47	DITH
48	GND
49	NC
50	NC

### 3. PIN DESCRIPTION

FPC Connector is used for the module electronics interface. The recommended model is FH12A-50S-0.5SH manufactured by Hirose.

No.	Symbol	Function
1	LED-A	Power for LED backlight (Anode)
2	LED-A	Power for LED backlight (Anode)
3	LED-K	Power for LED backlight (Cathode)
4	LED-K	Power for LED backlight (Cathode)
5	GND	Power ground
6	VCOM	Common voltage
7	VDD	Digital Power
8	MODE	DE/SYNC mode select. Normally pull high H: DE mode. L: HSD/VSD mode
9	DE	Data Input Enable
10	VS	Vertical sync input. Negative polarity
11	HS	Horizontal sync input. Negative polarity
12	B7	Blue data(MSB)
13	B6	Blue data
14	B5	Blue data
15	B4	Blue data
16	B3	Blue data
17	B2	Blue data
18	B1	Blue data
19	B0	Blue data(LSB)
20	G7	Green data(MSB)
21	G6	Green data
22	G5	Green data
23	G4	Green data
24	G3	Green data
25	G2	Green data
26	G1	Green data
27	G0	Green data(LSB)
28	R7	Red data(MSB)
29	R6	Red data
30	R5	Red data
31	R4	Red data
32	R3	Red data
33	R2	Red data
34	R1	Red data
35	R0	Red data(LSB)
36	GND	Power Ground
37	DCLK	Dot data clock
38	GND	Power Ground



39	L/R	Left or Right Display Control
40	U/D	Up / Down Display Control
41	VGH	Positive Power for TFT
42	VGL	Negative Power for TFT
43	AVDD	Analog Power
44	RESET	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10K $\Omega$ , C=1 $\mu$ F)
45	NC	No connection
46	VCOM	Common Voltage
47	DITHB	Dithering setting:DITHB=" H" 8bit resolution(default setting) DITHB=" L" 6bit resolution(last 2 bit of input data truncated)
48	GND	Power Ground
49	NC	No connection
50	NC	No connection

## 4. ELECTRICAL CHARACTERISTICS

### 4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Digital Supply Voltage	VDD	-0.3	5.0	V	
Analog Supply Voltage	AVDD	-0.5	13.5	V	
Gate On Voltage	VGH	-0.3	42	V	
Gate Off Voltage	VGL	-20	0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	12	40	V	

## 4.2 TFT LCD MODULE

### 4.2.1 Operating Conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	
Analog Supply Voltage	AVDD	9.4	9.6	9.8	V	
Gate On Voltage	VGH	17	18	19	V	
Gate Off Voltage	VGL	-7	-6	-5	V	
Common Voltage	VCOM	3.1	3.3	3.5	V	Note1
Logic Input Voltage	VIH	0.7VDD	-	VDD	V	
	VIL	GND	-	0.3VDD	V	

Note1: Please adjust VCOM to make the flicker level be minimum

Note2: TYP VCOM is only reference value. It must be optimized according to each LCM. Be sure to use VR and OP buffer on VCOM output. Please adjust VCOM to make the flicker level be minimum for getting excellent image.

### 4.2.2 Current Consumption

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Gate on Current	IVGH	VGH=18 V	-	(0.5)	-	mA	Note1
Gate off Current	IVGL	VGL=-6 V	-	(4.21)	-	mA	Note1
Digital Current	IVDD	VDD= 3.3V	-	(10.8)	-	mA	Note1
Analog Current	IAVDD	AVDD= 9.6 V	-	(27.26)	-	mA	Note1

Note1: Typ. specification : Gray-level test Pattern

Max. specification : Black test Pattern



(a) Gray-level Pattern



(b) Black Pattern



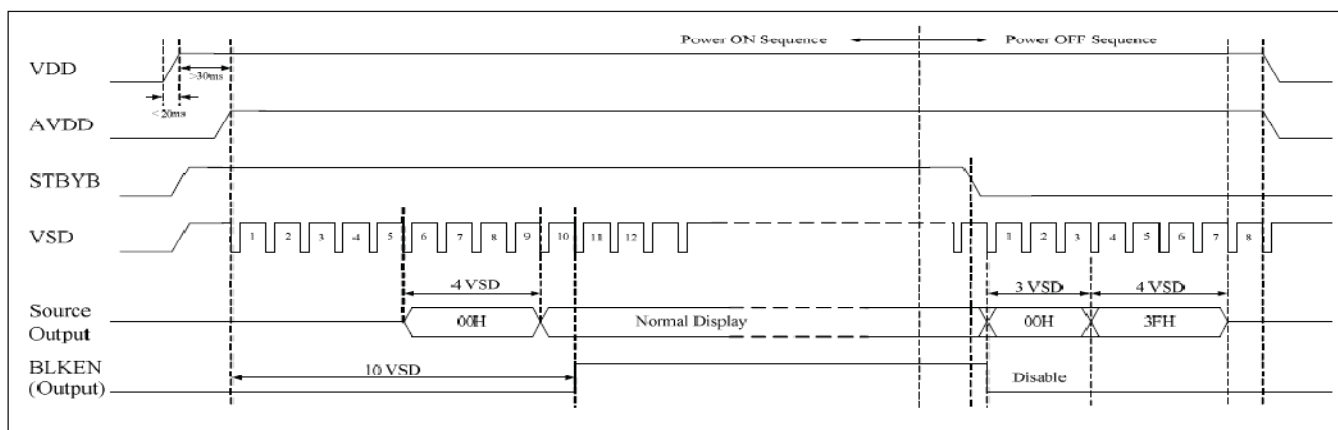
## 4.3 POWER、 SIGNAL SEQUENCE

To prevent the device damage from latch up, the power on/off sequence shown below must be followed.

Power ON: VDD, VSS → AVDD, VSSA → V1 to V14

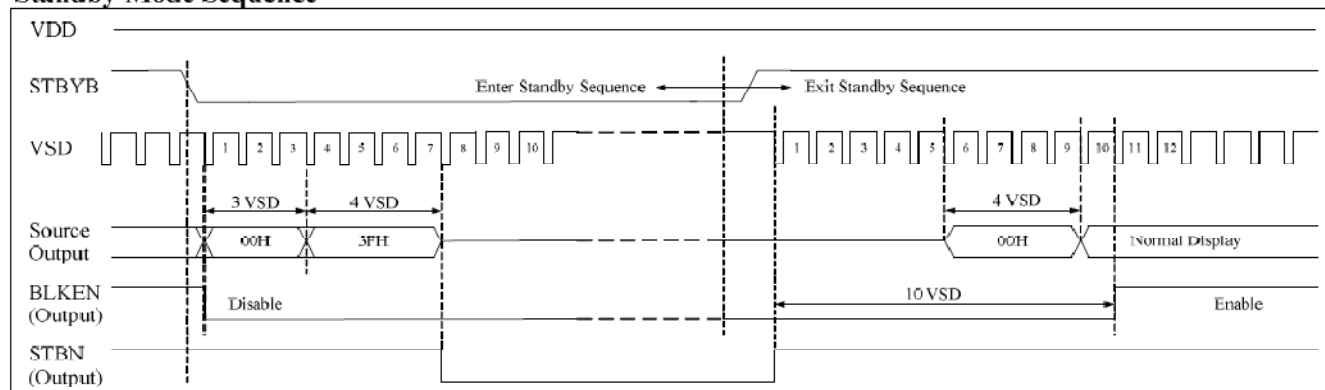
Power OFF: V1 to V14 → AVDD, VSSA → VDD, VSS

### 4.3.1 Power on/off control



### 4.3.2 Enter and exit standby mode sequence

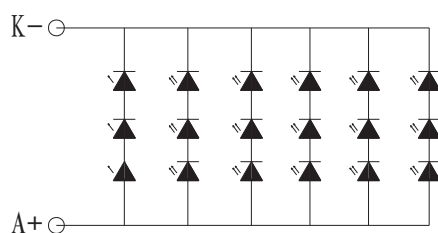
#### Standby Mode Sequence



#### 4.4BACKLIGHT UNIT

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
LED Current	Iled	-	120	-	mA	Total LED
Forward voltage	VF	9.0	9.6	10.5	V	IF=120mA
Reverse current	IR	-	-	50	μA	VR=5V,1LED
Power dissipation	Pd	1152			mW	Total LED
Peak forward current	IFP	100			mA	1LED
Reverse Voltage	VR	5			V	1LED

#### ※1. Internal Circuit Diagram



$$IF=120mA, 3 \times 6=18$$

## 5.INPUT SIGNAL TIMING

### 5.1DC electrical characteristics (VSS=0V, TA=25℃)

Parameter	Symbol	Spec.			Unit	Conditio n
		Min.	typ.	Max.		
Powersupplyvoltage	VDD	2.7	3.3	3.6	V	-
Power supply voltage	VDDA	6.5	-	13.5	V	-
Low level input voltage	VIL	0	-	0.3VDD	V	For digital circuit
High level input voltage	VIH	0.7VDD	-	VDD	V	For digital circuit
Output low voltage	VOL	-	-	VSS+0.4	V	IOL=400μA
Output high voltage	VOH	VDD-0.4	-	-	V	IOH=-400μA
Pull low/high resistance	Ri	200	250	300	kΩ	For the digital input pin @VDD=3.3V
Input leakage current	Ii	-	-	±1	uA	For digital circuit
Digital Operation current	Idd	-	5	14	mA	Dual gate mode or Cascade modeslave, Fclk=50MHz, LD=48KHzVDD=3.3V, CABC disable, Noload
		-	7	16	mA	Cascade mode master, Fclk=50MHz, LD=48KHz, VDD=3.3V, CABCdisable, Noload
Digital stand-by current	Ist1	-	10	50	μA	Clock & all functions are stopped
Analog Operating current	Idda	-	6	8	mA	Noload, Fclk=50MHz, FLD=48 KHz=@VDDA=10V, V1=8V, V14=0.4V
Analog Stand-by current	Ist2	-	10	50	μA	No load, clock & all functions are stopped
Input level of V1~V7	Vref1	0.4VDDA	-	VDDA-1	V	Gamma correction voltage input
Input level of V8~V14	Vref2	0.1	-	0.6VDDA	V	Gamma correction voltage input
Output Voltage deviation	Vod1	-	±20	±35	mV	Vo=VSSA+0.1V~VSSA+0.5V & Vo=VDDA-0.5V~VDDA-0.1V
Output Voltage deviation	Vod2	-	±15	±20	mV	Vo=VSSA+0.5V~VDDA-0.5V
Output Voltage Offset between Chips	Voc	-	-	±20	mV	Vo=VSSA+0.5V~VDDA0.5V
Dynamic Range of Output	Vdr	0.1	-	VDDA-0.1	V	SO1~SO1200
Sinking Current of Outputs	IOLy	80	-	-	μA	SO1~SO1200; Vo=0.1V vs.1.0V, VDDA=13.5V
Driving Current of Outputs	IOHy	80	-	-	μA	SO1~SO1200;Vo=0.1Vvs.12.5V, VDDA=13.5V
Resistance of Gamma Table	Rg	0.7*Rn	1.0*Rn	1.3*Rn	Ω	Rn: Internal gamma resistor

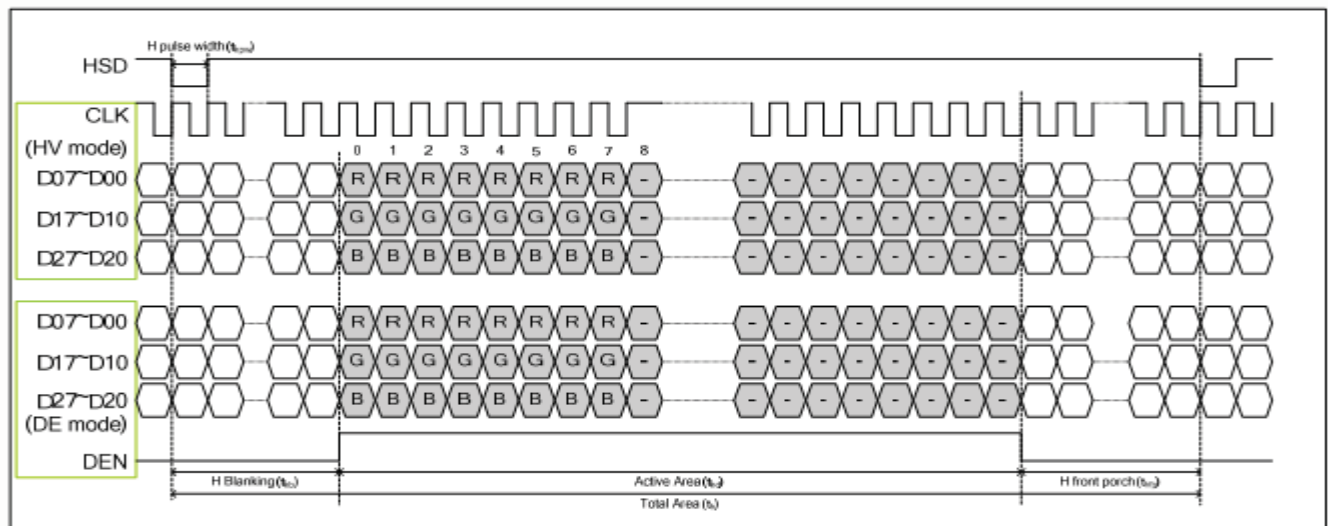
## 5.2 AC electrical characteristics

Parameter	Symbol	Spec.			Unit
		Min.	typ.	Max.	
HS setup time	$T_{hst}$	8	-	-	ns
HS hold time	$T_{hhd}$	8	-	-	ns
VS setup time	$T_{vst}$	8	-	-	ns
VS hold time	$T_{vhd}$	8	-	-	ns
Data setup time	$T_{dsu}$	8	-	-	ns
Data hold time	$T_{dhd}$	8	-	-	ns
DE setup time	$T_{esu}$	8	-	-	ns
DE hold time	$T_{ehd}$	8	-	-	ns
VDD Power On Slew rate	$T_{POR}$	-	-	20	ms
RSTB pulse width	$T_{Rst}$	10	-	-	us
CLKIN cycle time	$T_{cph}$	20	-	-	ns
CLKIN pulse duty	$T_{cwh}$	40	50	60	%
Output stable time	$T_{sst}$	-	-	6	us

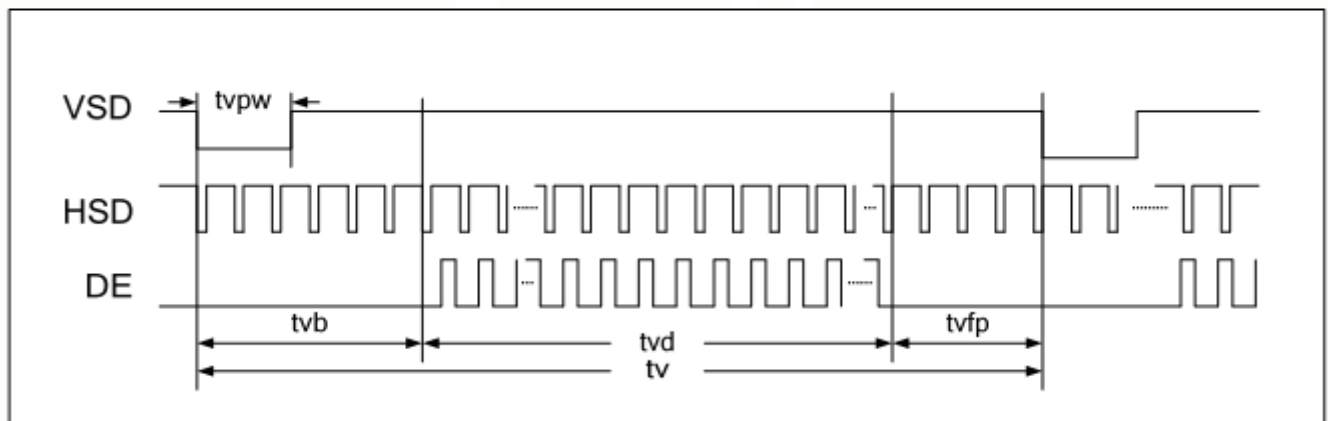
## 5.3 DATA INPUT FORMAT

### 5.3.1 TTL mode data input format

#### Horizontal timing



#### Vertical timing



### 5.3.2DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd	1024			DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd	600			T <sub>H</sub>
VSD Period	tv	610	635	800	T <sub>H</sub>
VSD Blanking	tvbp+ tvfp	10	35	200	T <sub>H</sub>

### 5.3.3 HV mode

#### Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	typ.	Max.	
Horizontal Display Area	thd	1024			DCLK
DCLK frequency	fclk	40.8	51.2	67.2	MHz
One Horizontal Line	th	1200	1344	1400	DCLK
HS pulse width	thpw	1	-	140	DCLK
HS Back Porch (Blanking)	thb	160			DCLK
HS Front Porch	thfp	1	160	255	DCLK

#### Vertical timing

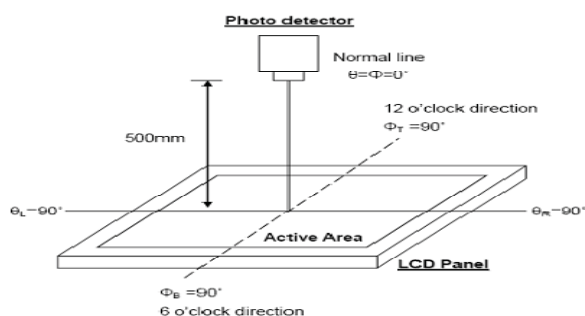
Parameter	Symbol	Spec.			Unit
		Min.	typ.	Max.	
Vertical Display Area	tvd	600			T <sub>H</sub>
VS period time	tv	624	635	750	T <sub>H</sub>
VS pulse width	tvpw	1	-	20	T <sub>H</sub>
VS Back Porch (Blanking)	tvb	23			T <sub>H</sub>
VS Front Porch	tvfp	1	12	127	T <sub>H</sub>

## 6. OPTICAL CHARACTERISTICS

$T_a = 25 \pm 2^\circ\text{C}$

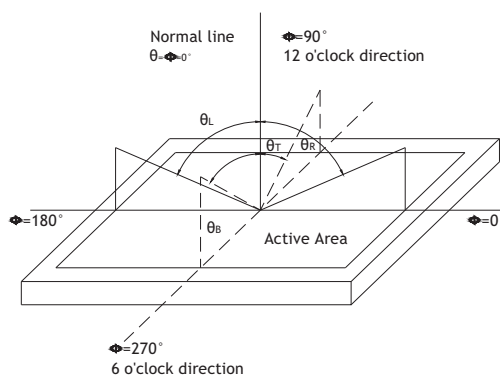
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Response time		Tr +Tf	Point-9	-	25	35	ms	Note1 Note3
Contrast ratio		CR		-	300	-	-	Note1 Note4
Color Chromaticity	White	X	$\theta=0^{\circ}$	0.234	0.284	0.334		Note1 Note5 Note7
		Y		0.268	0.318	0.368		
	Red	X		0.510	0.560	0.610		
		Y		0.280	0.330	0.380		
	Green	X		0.283	0.333	0.383		
		Y		0.557	0.607	0.657		
	Blue	X		0.102	0.152	0.202		
		Y		0.045	0.095	0.145		
Luminance		L		230	280	-	cd/m2	Note1 Note6 Note7
Luminance uniformity		YU		70	75	-	%	
Viewing Angle	Up.	$\theta$	Point-9 $CR \geq 10$	-	30	-	°	Note2
	Down.	$\theta$		-	50	-		
	Left.	$\emptyset$		-	60	-		
	Right.	$\emptyset$		-	60	-		
NTSC					50		%	

Note1: Definition of optical measurement system (BM-7)



Note2: Definition of viewing angle range and measurement system

Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).



### Note3: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photodetector output intensity changed from 10% to 90%.

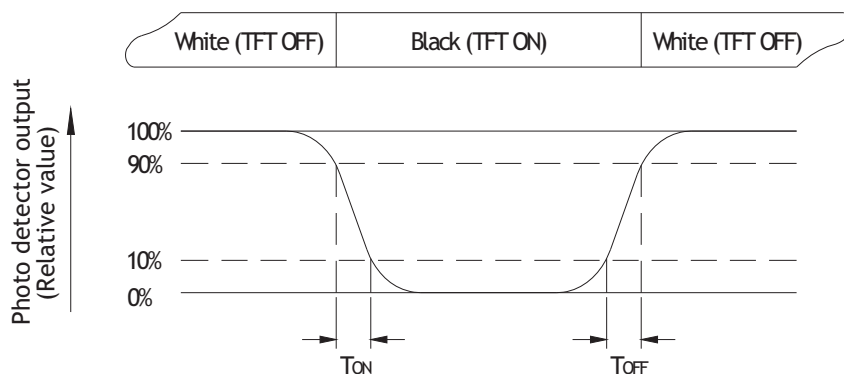


Fig. 6-3 Definition of response time

### Note4: Definition of contrast ratio

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD on the Whitestate}}{\text{Luminance measured when LCD on the Blackstate}}$$

“White state “: The state is that the LCD should drive by Vwhite.

“Black state”: The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

### Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

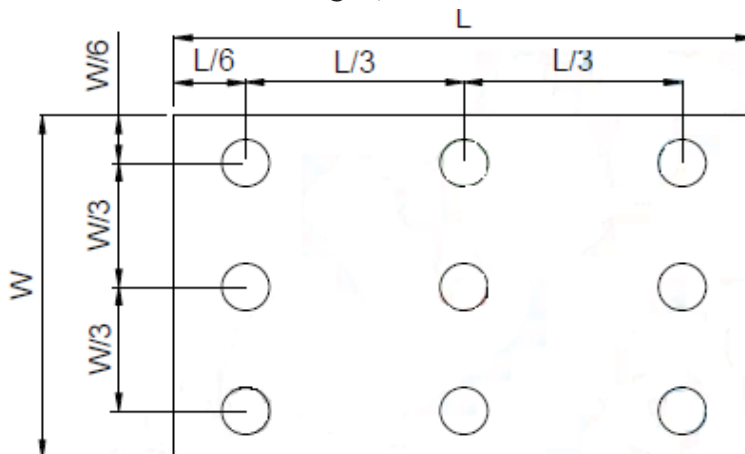
Note6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is IL=100mA

### Note7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas. Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity (U)} = L_{\min} / L_{\max}$$

L---Active area length, W---- Active area width



Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

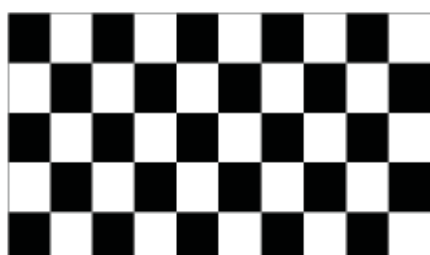
## 7.QUALITY ASSURANCE SYSTEM

### 7.1 TEMPERATURE AND HUMIDITY

Test Item	Test Condition	Remark
HighTemperatureStorage	Ta=60℃; 240hrs	IEC60068-2-1 : 2007 GB2423.2-2008
Low Temperature Storage	Ta=-10℃; 240hrs	IEC60068-2-1 : 2007 GB2423.1-2008
High Temperature Operation	Ta=50℃ , 240Hrs	IEC60068-2-1 : 2007 GB2423.2-2008
LowTemperatureOperation	Ta=0℃; 240hrs	IEC60068-2-1 : 2007 GB2423.1-2008
HighTemperatureHighHumidity Operation	Ta=40℃ , 80%RH , 120Hrs(no condensation)	IEC60068-2-78 : 2001 GB/T2423.3-2006
Thermal Shock	-10℃ (0.5h) ~ 60℃ (0.5h) / 100cycles	Startwith cold temperature , End with high temperature , IEC60068-2-14:1984,GB2423.22-2002
Image Sticking	25℃ ; 4hrs	Note1

Note1:Condition of image sticking test :25℃±2℃

Operation with test pattern sustained for 4hrs,then change to gray pattern  
immediately.after5 mins,themura must be disappeared completely



(a) Test Pattern (chess board Pattern )



(b) Gray Pattern

### 7.2 VIBRATION&SHOCK

Test item	Conditions	Remark
Packing Shock (non-operation)	980m/s <sup>2</sup> ,6ms, ±x,y,z 3times for direction	IEC60068-2-27 : 1987 GB/T2423.5-1995
Packing Vibration (non-operation)	Frequency range:10 HZ~50HZ Stroke:1.0mm,sweep:10 HZ ~50HZ x,y,z 2 hours for each direction	IEC60068-2-32 : 1990 GB/T2423.8-1995

### 7.3ESD

Test item	Conditions	Remark	
Electro Static Discharge Test (non-operation)	150pF , 330Ω , Contact:±4KV,Air:±8KV	1	Class B
	200pF , 0Ω , ±200V contact test	2	

Note: Measure point :

1. LCD glass and metal bezel
2. IF connector pins





3.ESD class B:some performance degradation allowed. Self-recoverable.  
No data lost,no hardware failures.

## **8. GENERAL PRECAUTION**

### **8.1 SAFETY**

1. Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
2. If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
3. If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

### **8.2 STORAGE CONDITIONS**

1. Store the panel or module in a dark place where the temperature is  $23\pm5^{\circ}\text{C}$  and the humidity is below  $50\pm 20\%\text{RH}$ .
2. Store in anti-static electricity container.
3. Store in clean environment, free from dust, active gas, and solvent.
4. Do not place the module near organics solvents or corrosive gases.
5. Do not crush, shake, or jolt the module.

### **8.3 HANDLING PRECAUTIONS**

1. Avoid static electricity which can damage the CMOS LSI.
2. The polarizing plate of the display is very fragile. So, please handle it very carefully.
3. Do not give external shock.
4. Do not apply excessive force on the surface.
5. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
6. Do not use ketonic solvent & Aromatic solvent, use with a soft cloth soaked with cleaning naphtha solvent.
7. Do not operate it above the absolute maximum rating.
8. Do not remove the panel or frame from the module.
9. When the module is assembled, it should be attached to the system firmly, Be careful not to twist and bend the module.
10. Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.
11. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth in case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

### **8.4 WARRANTY**

1. The period is within twelve months since the date of shipping out under normal using and storage conditions.
2. Do not repaired or modified the LCM. It may cause function to lose efficacy, Starry does not warrant the LCM.
3. All process and material comply ROHS.

[illegible]